Amendment to Response
to May 17th 95 RFP #11

Mr. Deeam 3495

Exhibit E

OFGS File No.: IR 2.064 (2-838)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:

ALEXANDER LIDOW et al.

Patent No.: 5,008,725

Reexamination Control No.: 90/003,495

Filing Date: July 15, 1994

Examiner: CARROLL, J.

Group Art Unit: 2508

RESPONSE PURSUANT TO
37 C.F.R. § 1.550(b)

Box Reexam
Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Sir:

This is responsive to the Office Action mailed May 17, 1995 (Paper No. 11) rejecting independent claims 3, 7 and 8 (and certain claims dependent thereon) of U.S. Patent No. 5,008,725 (hereafter "the '725 patent"), as amended by the Amendment filed March 24,

1995.[1] For the reasons set forth below, reconsideration of the rejections is respectfully requested.

I. INTRODUCTION.

In response to the Amendment filed March 24, 1995, the Examiner, in the Office Action mailed on May 17, 1995, withdrew all rejections based upon the Takakuwa and Hendrickson documents as primary references. The Examiner, however, concluded that

> "Given the diminished status of the Takakuwa reference and the Hendrickson Patent as formerly plausible prior art information against the presently amended Patent Claims, we find that the Okabe et al. reference remains an applicable alternative." (5/17/95 Office Action, p. 8.)

The Examiner introduced new rejections of independent claims 3, 7 and 8, relying upon Okabe as a primary reference.

Patent Owner's prior discussion of the Okabe reference was limited due to Okabe's relatively modest role in the original rejections. The present response expands upon the previous discussion and presents additional reasons (supported in the prior art and by the attached Declaration of John Shott) demonstrating that Okabe is not relevant to the high power MOSFET invention claimed in the '725 patent, and would not have suggested the claimed invention to one of ordinary skill in 1979. Additionally, Patent Owner comes forward in this Response with additional evidence, in the form of a second Declaration of Alexander Lidow, demonstrating the nexus between the commercial success of spaced base cellular power MOSFETs and the invention claimed in the '725 patent.

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[1] The Non-Responsive Amendment of May 25, 1995 returned independent claims 3, 7 and 8 to their pre-amendment form (*i.e.*, they are now identical to those claims in the previously issued reexamination certificate) and added new claims 18, 22 and 25 corresponding, respectively, to amended claims 3, 7 and 8.

II. THE OKABE REFERENCE HAS NO TEACHINGS APPLICABLE TO A HIGH POWER MOSFET.

Okabe, in introducing his invention, states that there are two kinds of prior art FET devices: the then conventional JFET of Fig. 1 and the then conventional MOSFET of Fig. 2. He then shows how his new advance improves the performance of the JFET of Fig. 1 by liberalizing a design trade-off. Thus, the principal engineering problem addressed by Okabe concerns the tradeoff between on- and off-condition performance -- *i.e.*, design choices which are made to improve the current-handling capability in the on condition will degrade the ability of Okabe's signal level (8 to 10 volts) JFET of Fig. 1 to "pinch off" current and turn the device off. Note that this trade off does not relate to the MOSFET of Fig. 2, since the device is turned-off by removing the channel (*i.e.*, the inversion layer) from under the insulated gate.

As illustrated in Figure A, Okabe discusses operating the JFET in the on condition so that electrons "flow[ ] from the source 3 via the gate region 2 to the drain electrode 6" (USPTO Trans., p. 1):

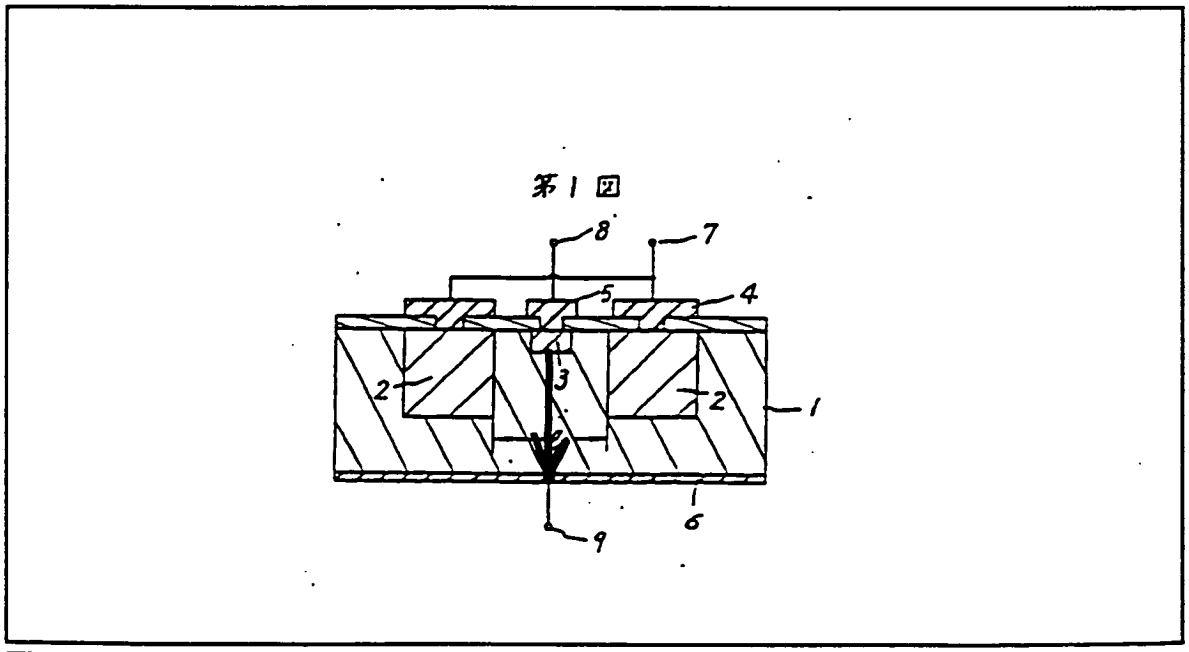

Figure A: Okabe Fig. 1 annotated to show electron flow in the on condition.

Similarly, as illustrated in Figure B, the JFET can be turned off by creating a depletion region between the gate regions to "pinch off" electron flow: "an electron's passage (hereinafter called a channel) is opened/closed by means of a depletion layer made between the region 2 and the substrate 1" (USPTO Trans., p. 1):

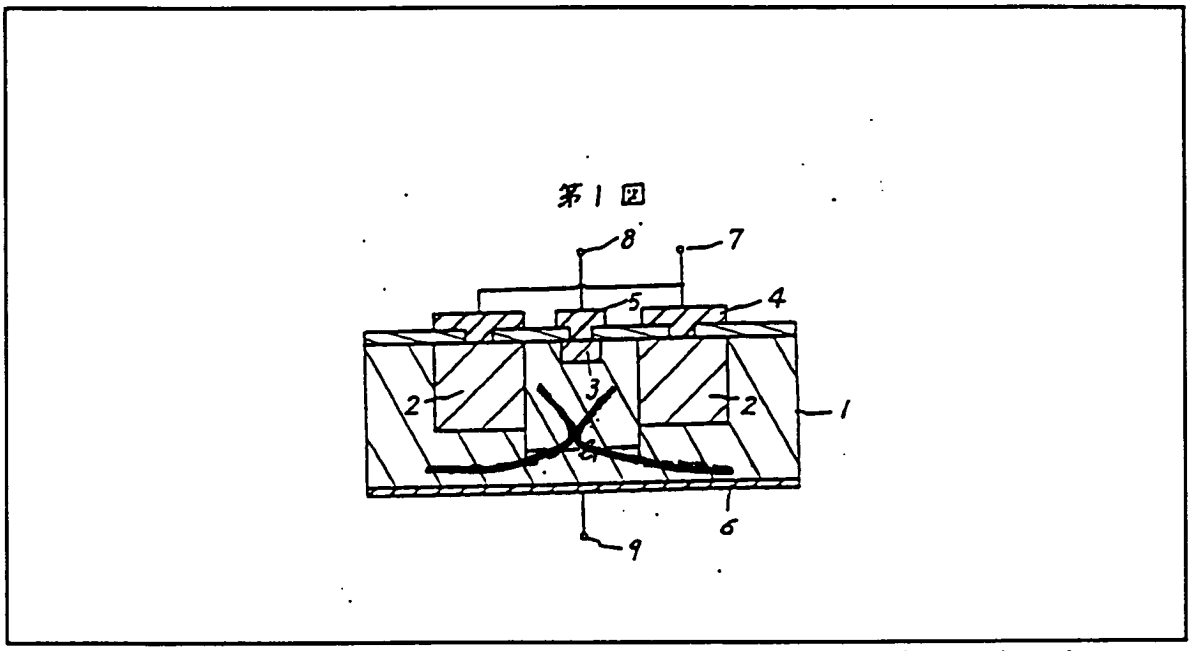

Figure B: Okabe Fig. 1 annotated to show channel and depletion regions in "pinch off" condition.

The Okabe translations of record are clear concerning the conditions that determine the pinch-off state. Here is a comparison of the three translations of record:

Liu Translation	Morikami Translation	USPTO Translation
The condition of pinch-off is determined by gate voltage, drain voltage, the distance l between gate zones, and the impurities in the substrate.	The pinch-off state is determined by gate voltage, drain voltage, the distance between the gate regions, l, and impurity concentration in the substrate.	The state of the pinch-off is controlled by the distance ℓ_1 between the gate region and the voltage/drain voltage and by the substrate impurities concentration level.

The next sentence however seems to be garbled in the Liu and Morikami translations, but is coherently rendered in the USPTO translation: "More specifically, [the] longer the distance ℓ_1 is, or the higher the substrate impurities concentration is, the harder it is to reach the pinch-off state." (USPTO Trans., p. 2.) Thus, making the channel wider (*i.e.*, increasing

the distance ℓ_1 between JFET gate regions) or increasing the conductivity (*i.e.*, decreasing the resistance) at the drain side of the channel to improve on-state performance will make it more difficult to achieve pinch-off -- *i.e.*, improving on-state performance will make it more difficult to turn the device off.

Note that the above discussion to this point has no application to a MOSFET. Further, the above discussion is independent of the surface expression of the Okabe gate regions -- *i.e.*, it could apply to the "conventional linear type" of JFET structure Okabe refers to (on page 3 of the USPTO translation), where apparently (as illustrated in Figure C) one or more source stripes are disposed between elongated gate regions 2:

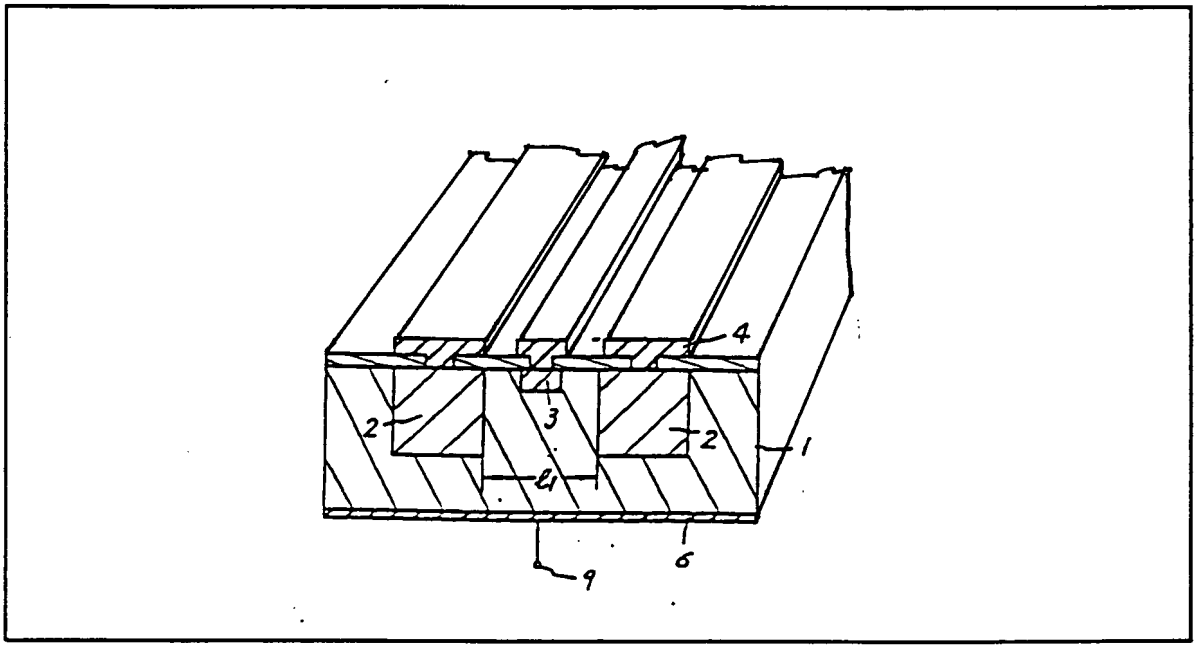

Figure C: "Conventional linear type" JFET employing Okabe Fig. 1 cross section.

Okabe, of course, described an improvement over this "conventional linear type" -- making a two-dimensional array of gate regions, as illustrated in Okabe Fig. 3. This improvement, however, had a potential drawback in that the regions at the intersections of the diagonals between adjacent gate regions could be more difficult to pinch off, again raising a potential tradeoff with on-state performance:

"To deplete this region, the larger drain voltage is required or the gate region distance ℓ_1 needs to be made shorter. Making the ℓ_1 shorter means to make the channel narrower, but this will make the current smaller [and] therefore is not desirable. The device which does not go into the pinch-off state without raising the [drain voltage] is not desirable due to its large loss." (USPTO Trans., p. 2.)[2]

Okabe attempts to minimize this potential JFET-related drawback by staggering the rows of gate regions, as shown in Fig. 4. Okabe reports that this arrangement permits him to increase "channel width" over the "conventional linear type" JFET 1.5 times for a given chip size, while maintaining pinch-off at a drain voltage of -8 to -10 volts, summarizing his invention as "permitting the current level [to] be raised without drastically changing the pinch-off characteristic." (USPTO Trans., p. 3.)

The Okabe reference itself does not purport to directly apply this invention to the "conventional" MOSFET shown in cross section in Okabe Fig. 2, nor would one of ordinary skill in 1979 have any motivation to employ a JFET improvement in a MOSFET. For example, when discussing Figs. 3 and 4 showing the JFET array in top view, Okabe consistently refers to the replicated structures as "gate regions"; they are never called a MOSFET base or even the "low impurity concentration" region 10. In addition, the electrode structure of Fig. 2 depicts some form of annular (or elongated annulus) structure; it is inconsistent with an array of replicated bases. Indeed, as the Examiner has confirmed, "The Patent Owner reasonably and correctly concludes that the Figure 2 MOSFET gate arrangement is . . . inconsistent with a MOSFET array having spaced base regions." (5/17/95 Office Action, p. 10.)

The question therefore arises whether Okabe suggests to those of skill that the "conventional" MOSFET of Fig. 2 could be modified and then replicated (like the JFET gate regions in Okabe Fig. 3 or 4) in order to arrive at the high power MOSFET claimed in the

[2] This quote substitutes the phrase "drain voltage" for "current" in the USPTO translation. The translation of "current" does not make sense, and, moreover, both the Liu and Morikami translations use the phrase "drain voltage."

'725 patent, i.e. a high power MOSFET comprising "a plurality of symmetrically disposed laterally distributed polygonal base regions." Patent Owner respectfully submits that Okabe made no such suggestion.

In the latest Office Action, the Examiner states:

> "In a brief reference to Figure 2 on translation page 2 we find evidence in the following excerpt that Okabe et al. would have disagreed with the Patent Owner's assertion [that Okabe does not suggest that low impurity concentration region 10 in Fig. 2 could be arranged analogously to JFET gate regions 2 of Fig. 1 in an array after Figs. 3 or 4].
>
> 'The field effect transistor shown in Fig. 2 also shows the analogous relationship.'"

(5/17/95 Office Action, p. 9.)

The Patent Owner respectfully submits that the Examiner is reading an aside by Okabe out of context. Okabe, in passing, analogizes Fig. 2 to Fig. 1 only in one limited respect -- *i.e.*, the pinch-off across distance ℓ_1 in JFET Fig. 1 is analogously found across distance ℓ_2 in FET Fig. 2:

> "The state of pinch-off [in JFET Fig. 1] is controlled by distance ℓ_1 between the gate region and the voltage/drain and by the substrate impurities concentration level. More specifically, the longer the distance ℓ_1 is, or the higher the substrate impurities concentration is, the harder it is to reach the pinch-off state. The field effect transistor shown in Fig. 2 also shows the analogous relationship." (USPTO Trans., p. 2.)

However, this is a "parasitic" JFET in Fig. 2 and is not employed to turn-off the MOSFET. This is accomplished by the conventional MOS gate in Fig. 2. Okabe does not state or suggest (let alone explain how) the MOSFET of Fig. 2 might be employed analogously to the JFET of Fig. 1 in the topological arrangements of Figs. 3 or 4. Nor does Okabe state or suggest that the FET of Fig. 2 could be operated as a *power* transistor, as distinguished from the signal level JFET of Fig. 1.

Further, even though the Examiner acknowledges that "[t]he Patent Owner reasonably and correctly concludes that the Figure 2 MOSFET gate arrangement [with gate electrode 11 only on the inner surface of region 10] is [ ] inconsistent with a MOSFET array having spaced base regions," the Examiner nonetheless concludes that

> "understanding that Okabe et al. expected one to distribute analogous MOSFET base regions (10) in either conventional or staggered array fields to achieve a desirably large channel width, after
>
> > '[. . .] since a size of the current is in proportion with a channel width, it is desirable to have a large channel width on the same plane.',
>
> excerpted from translation page 2, we perforce conclude that one would have possessed sufficient common knowledge and common sense to have formed gate electrode (11) to surround each base region so as not to throw away potential channel width that Okabe et al. clearly and unambiguously intended to make large." (5/17/95 Office Action, p. 10, ellipsis in original.)

Again, Patent Owner respectfully submits that the Examiner is reading more into Okabe than justified by its text or by the understanding of a person of ordinary skill at the relevant time. The statement from Okabe quoted by the Examiner is made explicitly with reference to Okabe's JFET. Channel width in a JFET is not the same as channel width in the MOSFET of the '725 patent. Channel width in JFET Fig. 3, for example, is comprised of the distances ℓ_1 between JFET gates (USPTO Trans., p. 2), while channel width in the '725 MOSFET base array is measured by the perimeter of the bases at the device surface. Again, turn-off of the MOSFET of Fig. 2 is accomplished by removing the gate signal, not by pinching off the parasitic JFET. Thus, the thrust and purpose of Okabe's improvement, which is to allow higher forward current while still being able to pinch-off the JFET, is wholly inapplicable to a MOSFET.

Putting to one side the design tradeoffs associated with off-state performance, a JFET designer wants large "channel width" -- *i.e.*, large distances between opposing gate regions -- in order to reduce the resistance to current flow between the source and drain electrodes in the on condition. Extending this concept to two dimensions, the JFET designer

wants to maximize the portion of the chip surface dedicated to the source, as opposed to the portion of the surface dedicated to the gate regions -- *i.e.*, for a given chip size, the more of the chip that is in contact with the source electrode, the lower the resistance between source and drain. The MOSFET designer, on the other hand, wants to maximize the linear distance corresponding to the total perimeter length of the bases arranged on a given chip surface area. Put another way, the JFET designer seeks to maximize the source *area* per unit chip area (or, equivalently, to minimize gate area per unit chip area), while the MOSFET designer seeks to maximize channel width (peripheral length) per unit chip area. Thus, for example, while increasing the distance between JFET gates arranged in an array will (as Okabe explains) increase JFET channel width (USPTO Trans., p. 2), increasing the distance between MOSFET bases in an array will *decrease* channel width per unit area of silicon because the number of bases or the size of the bases will have to be correspondingly reduced.

As noted, the foregoing discussion ignored the possible effects increasing channel width might have on off-state performance. As the Examiner is well aware, however, the design tradeoffs between on- and off-state performance present some of the most difficult issues faced by transistor designers. Indeed, Okabe discusses at length design trade-offs necessary to balance JFET on-state performance with JFET off-state performance. Okabe, however, makes no comment on the very different design trade-offs necessary to balance MOSFET on-state and off-state performance, and in particular says nothing about design trade-offs relevant to the design of *power* MOSFETs. Indeed, as discussed in the next section, two of the three Okabe co-inventors specifically confronted the challenge of improving MOSFET current handling by increasing channel width per unit area while at the same time increasing MOSFET breakdown voltage and did not arrive at the solution of the '725 patent. Instead, the Okabe co-inventors went in precisely the opposite direction.

III. THE OKABE INVENTORS THEMSELVES ADDRESSED THE ISSUE OF CHANNEL WIDTH IN A POWER MOSFET AND ARRIVED AT A SOLUTION OPPOSITE TO THAT CLAIMED IN THE '725 PATENT AND SUPPOSEDLY SUGGESTED BY THE OKABE REFERENCE.

As reflected in the Liu and Morikami translations, there were three co-inventors of the Okabe invention: Yasuaki Okabe, Isao Yoshida and Shikayuki Ochi of Hitachi Ltd. The Okabe patent application was filed on March 1, 1976, essentially simultaneously with the February 1, 1976 submission and April 15, 1976 revision of the manuscript for the article entitled "A High Power MOSFET with a Vertical Drain Electrode and a Meshed Gate Structure" (published in the August 1976 issue of the IEEE Journal of Solid-State Circuits, starting at page 472) whose co-authors include two of the three Okabe co-inventors: Isao Yoshida and Shikayuki Ochi of the Central Research Laboratory of Hitachi Ltd. This article is of record as Reference AO, and is usually referred to as the Yoshida IEEE reference.

Significantly, Yoshida and his co-authors note at the outset of their article that

> "The major problem in realizing power MOSFET's is their low current handling capability and relatively low breakdown voltage. Various attempts have been made to improve the power handling capability of MOSFET's by making their channel widths larger and improving their breakdown voltages." (Yoshida IEEE, p. 472.)

Yoshida and his co-authors then go on to describe the design challenge of increasing current-handling capability in a MOSFET:

> "It is known that the drain current of a MOSFET is proportional to the channel aspect ratio . . . . Therefore, the problem is how to realize such a high aspect ratio in a given chip size." (Yoshida IEEE, p. 472.)[3]

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[3] It should be noted here that the channel "aspect ratio" refers to the "channel width" divided by the "channel length." In Yoshida's design the channel length is the distance between the edge of the gate and the highly conductive drain diffusion -- here, 8 μm.

(continued...)

Thus, Okabe co-inventors Yoshida and Ochi are striving in the Yoshida IEEE article to improve channel width per unit area in a power MOSFET, while at the same time improving breakdown voltage in the off condition.

The design choice explored in the Yoshida IEEE article is a meshed-gate structure in which a number of square P+ drain regions are formed in a "checkerboard" fashion in an N- epitaxial layer atop a P+ substrate (the drain diffusions penetrate the epitaxial layer, so the drain electrode can be placed on the bottom surface of the device) (Figure D-1, below). The gate oxide and a "meshed" polysilicon gate are then formed, such that alternate openings in the polysilicon contain a drain diffusion (with the openings spaced or "offset" from those diffusions by the 8 μm "channel length") (Figure D-2). Boron (P type) ions are then implanted between the gate edges and the drain regions to form the so-called channel regions (Figure D-3).[4] The sources are then formed in the remaining openings in the gate mesh, and the source electrode is formed over the top surface of the device (Figure D-4).[5]

This Yoshida IEEE MOSFET structure is vastly different from that supposedly suggested by the Okabe invention, much less that disclosed and claimed in the '725 patent:

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[3](...continued)
Channel width, on the other hand, is the total distance along the top surface of the channel -- a quantity that will depend on the total chip area and the efficiency with which channel can be packed into a given area. Yoshida reports that his design achieved 94 cm of channel width (*i.e.*, an aspect ratio of about 1.2 x 10^5) on a 5 mm^2 chip, which he reports represents "twice the channel aspect ratio per unit area of conventional MOSFET's with the same channel length." (Yoshida IEEE, p. 472.)

[4] Unlike the channels in the '725 power MOSFETs, the Yoshida "channels" are not the inversion layers underlying the gate electrode, but rather are the lightly doped region permitting conduction from the inversion layer to the drain region. This region in the Yoshida structure is also referred to as an extended drain region.

[5] Yoshida reports that the drain current of his design "reaches as high as 20 A" and that "A breakdown voltage of 100V is obtained due to the ion implanted offset gate structure, which is twice that of a conventional device." (Yoshida IEEE, p. 474.)

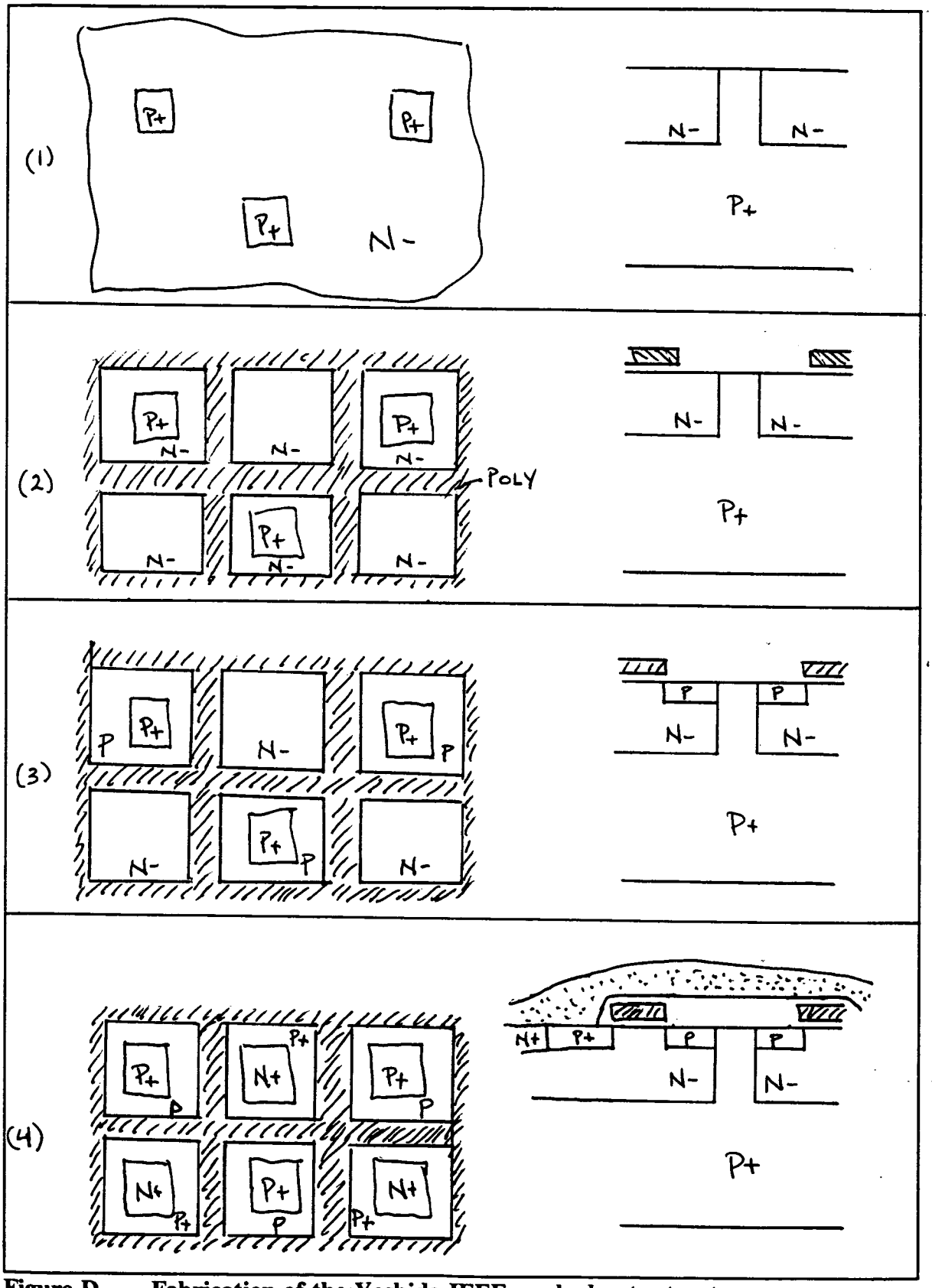

Figure D. Fabrication of the Yoshida IEEE meshed gate structure.

- The Yoshida IEEE structure employs a **single base** (penetrated by discrete drain "pedestals"), not spaced, polygonal bases defining a "continuous and uninterrupted" common conduction region or lattice of drain material, as required by the pending claims.

- The Yoshida IEEE structure is comparable to a lateral-conduction device, where the drain current flows laterally along the top surface of the device under the full width of the gate electrode (and then through the shallow extended or "offset" drain structure). The '725 structure, in contrast, is a true vertical-conduction device because the drain current, upon exiting the channel, is directed vertically between the spaced bases.

- The Yoshida IEEE structure employs an "offset gate structure" at the top surface of the device to support the drain voltage in the off condition -- *i.e.*, when the device is turned off, the drain region and P+ drain pedestals rise to the full 100 volts of drain voltage, with this voltage supported at the top surface by the lightly doped, 8-μm wide, P type offset drain regions. The '725 structure, in contrast, employs extremely short channels and supports the off-state drain voltage in the bulk of the device.

As evidenced by the direction taken by the Okabe co-inventors to increase channel width in their IEEE article, the '725 invention was not obvious to them from their own patent document. For this reason, Patent Owner respectfully disagrees with the Examiner's conclusion that a skilled practitioner reading the Okabe reference

> "would have possessed sufficient common knowledge and common sense to have formed [Okabe] gate electrode (11) to surround each base region so as not to throw away potential channel width that Okabe et al. clearly and unambiguously intended to make large. Thus, in transforming the MOSFET of Figure 2 into either array of Figures 3 and 4, one would have changed the gate (11) arrangement of Figure 2 so that the gate electrode would surround each and every base region in the array to make large the channel width." (5/17/95 Office Action, p. 10.)

The Patent Owner respectfully submits that the foregoing analysis is sufficient standing alone to show that the Examiner cannot be correct in his obviousness rejection, as two of the Okabe co-inventors -- simultaneously with the Okabe filing -- expressly addressed the design problem of increasing channel width per unit area in a power MOSFET and arrived at a solution that is completely different from that supposedly suggested by the Okabe reference. If the '725 invention -- the dominant topology of present-day high power MOSFETs -- were obvious from Okabe, then why did the Okabe co-inventors themselves proceed in a direction 180° away from the '725 invention? Indeed, as explained in the next section, because the power MOSFET design path dictated by the conventional wisdom of the time led away from the '725 invention, those of skill reading Okabe would no more have arrived at the '725 invention than did the Okabe co-inventors in their Yoshida IEEE article.

IV. OTHER REFERENCES BEFORE THE EXAMINER EXPLAIN THE TECHNOLOGICAL REASONS WHY OKABE DOES NOT SUPPORT THE READING SUGGESTED BY THE EXAMINER -- A READING AT ODDS WITH THE CONVENTIONAL WISDOM OF THE ART PRIOR TO THE '725 INVENTION.

Patent Owner respectfully submits that the references available to the Examiner explain the technological reasons why Okabe cannot support the reading suggested by the Examiner -- that reading conflicts with the conventional wisdom in the art at the time of the Okabe disclosure and prior to the '725 invention.

Prior to the 1978 invention of the '725 structure, as now, the challenge facing power MOSFET designers was how to pack as much channel width as possible into a given chip area while preserving the ability of the device to withstand comparatively high drain voltages in the off state. One of the principal modes of device failure in the off condition was then, as it is today, avalanche breakdown of the reverse-biased junction formed between the base and drain regions. Since in a typical application the base is grounded and the drain electrode is held at a relatively high voltage in the off condition, the junction between those two regions will be reverse-biased by many volts -- perhaps even hundreds of volts -- in the off condition. As described in the accompanying Declaration of John Shott, Ph.D., it was

well known in the art that, depending on the doping of the base and drain, the junction between them would experience a peak electric field that grew with increasing drain voltage, and at some point would achieve a critical field strength sufficient to cause avalanche of that junction.

It was also known that the surface expression of the diffused region would affect the breakdown voltage of the junction formed by that diffusion. Since all real-world junctions, being finite, have some curvature, designers concerned with breakdown had to take into account the effect this curvature might have on peak electric field strength and hence on breakdown voltage.

For example, as described in the Sze reference supplied by the Examiner, the junction formed by diffusion through a window is essentially planar along the bottom of the junction (*i.e.*, in the middle of the window), essentially cylindrical along the edges of the window and essentially spherical at the corners of the window. The electric-field and breakdown effects of these junction shapes are described by Sze as follows:

> "Since electric-field intensities are higher for cylindrical and spherical junction regions, the avalanche breakdown voltages of such regions can be substantially lower than that of a plane junction having the same background doping." (Sze, p. 402.)

Similarly, a textbook published in 1977 entitled *Semiconductor Power Devices*, by S.K. Ghandhi, also notes that the edge of a diffusion window will result in a cylindrical junction, where "for the same reverse voltage, the peak electric field is higher for the cylindrical junction [than for the planar junction]. Intuitively, therefore, we can expect the breakdown voltage to be lower in this case." (p. 59.) Similarly, Ghandhi observes that "for the same radius of curvature, the spherical junction has an even lower breakdown voltage than the cylindrical junction." (p. 63.) For these reasons, Ghandhi concludes that sharp corners in diffusion windows are to be avoided:

"Extremely small radii of curvature are encountered in sharp corner regions associated with masked diffusion through rectangular windows. Such corners must always be avoided by rounding them off; often designers of power devices use circular lateral geometry to avoid completely junction breakdown due to spherical curvature." (p. 63.)

This principle is also found in the references previously considered by the Examiner. In the Dingwall patent, for example, the inventor describes the prior art technique in lateral-conduction devices of using square drain diffusions at the top surface. Dingwall reports that "[b]y viewing operating [] devices through a microscope in the dark it has been shown that the corners of the enclosed drains 'light up' first, which means that avalanche starts at the drain corners." (col. 1, lines 26-29.) Dingwall's invention related to deliberately increasing or decreasing breakdown voltage by changing the shape of the drain. For example, Dingwall uses octagonal drain shapes to increase breakdown voltage by about 10%, and uses triangular drain shapes to decrease breakdown voltage by about 13%. (col. 2, lines 3-28.)

Additionally, as described more fully in the attached Declaration of John Shott, the junction-curvature effect on breakdown, particularly at corners, works in reverse when the corners are formed by an opening in the diffusion (such as with an annular diffusion). Thus, an annular junction would have better avalanche breakdown performance at the interior corners than would a polygonal diffusion at the exterior corners. This is why frame-base configurations (*i.e.*, bases with only interior corners and *inwardly* conducting channels) such as Ishitani and Takakuwa were felt to be superior for higher-voltage applications to solid-base configurations (with *outwardly* conducting channels).

Takakuwa was discussed extensively in the Patent Owner's Amendment of March 24, 1995. To summarize, that reference teaches that power MOSFET structures should avoid large drain voltages near the thin gate oxide, and describes two techniques for doing so: (1) with a base region having an *outwardly conducting* channel (i.e., the gate is disposed on the outer periphery of a solid base), the designer should include a separate surrounding ring diffusion that can be biased in parallel with the base to create a JFET to

support the voltage across the device in the off condition; or (2) in the alternative, the designer may eliminate the need for a separate JFET diffusion by using an annular or frame base with an *inwardly conducting* channel (*i.e.*, in this configuration, the gate lies atop the inner periphery of an opening within the base). As the Examiner has already concluded, neither of these configurations suggests the array of polygonal bases (with no separate JFET diffusions) claimed in the '725 patent. While Takakuwa does not explicitly address the issue of avalanche breakdown of the base-drain junction in either configuration, based on the foregoing discussion and as discussed in Dr. Shott's Declaration, those of skill understood that the annular base with the inwardly conducting channel would have reduced peak electric fields, and hence higher breakdown voltage, than the solid base with the outwardly conducting channel.

The Ishitani reference also takes advantage of inwardly conducting annular channel regions in a single base penetrated by drain "pedestals" within the annular channels: "The frame [base] region 23 can be formed in a mesh-like pattern having a plurality of through holes 23a . . . ." (Ishitani, col. 5, lines 1-3.) Again, although not explicitly discussed in the Ishitani reference, those of skill would understand that the base-drain junction would be curved so as to avoid avalanche breakdown at the corners of the "through holes."

A frame-base design is also discussed in the Hanes patent, which employs a single base with two parallel rows of finger-like openings where the drain material can reach the top surface of the device. The Hanes reference describes avalanche breakdown of the base-drain junction in the vicinity of those openings:

> "In operation of the power transistor of the present invention, adjacent p-regions, i.e., regions 71, are very closely spaced according to the teachings of the present invention. As the voltage across the transistor increases and the transistor is in the OFF state, the fields from adjacent p-n junctions meet and the horizontal components thereof oppose and cancel each other so that avalanche voltage is not unnecessarily lowered because of junction curvature." (col. 6, lines 53-61.)

Note that these long, fingerlike openings are in a single p type base region 71, with the junction curvature along these sides being essentially cylindrical. Hanes teaches that the width of these openings should be about 4 μm. (Figure 5.)

The Jambotkar reference describes a power MOSFET using a single line of parallel, finger-like base[6] regions surrounded by a separate ring-shaped diffusion. Jambotkar teaches that breakdown performance is improved by having very small distances between the parallel bases, and by having an unbiased diffusion surrounding all of the bases:

> "[An] outer unbiased annular P region is shown for improving the drain-to-[base] reverse breakdown voltage through reduction of electric field at the curvature of the outer periphery of the P [base] regions. The vicinity of the adjacent inner peripheries of the P [base] regions reduces the electric field near the curvature of the inner peripheries of the P [base] regions. . . . The FET [base] P diffusions are designed to be located apart from one another by very small distances, preferably between 4 and 10 micrometers. Further, unbiased or floating annular P diffusions are also designed to flank the outer peripheries of the P [base] diffusions 18. These P regions 16 are located preferably between about 20 to 50 micrometers apart. The close proximity of the adjacent [base] diffusions 18 reduces the electric field in the curvature regions of the inner peripheries of these P diffusion/N- body junctions, while the presence of the unbiased P diffusions 16 at the appropriate distance from the outer peripheries of the P [base] diffusions 18 reduces the electric field in the curvature region of the outer peripheries of those outer P [base] diffusions 18. As a consequence, the drain to [base] breakdown voltage is made practically equal to the maximum possible value which is the plane P to N- junction reverse breakdown value." (Jambotkar, col. 5, lines 18-52.)

Jambotkar thus teaches the use of essentially linear structures that minimizes corner effects (where junction curvature is higher than along the edges) and the use of some structure (either a closely spaced parallel base or a floating ring) to support the electric field along the base-drain junction. No suggestion is made in Jambotkar that these essentially linear structures (long, thin bases with linear sources) should be replaced by polygonal bases with annular sources, as in the '725 invention. Indeed, Jambotkar teaches away from the '725

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[6] Jambotkar refers to the P type regions in which the channels are formed as "substrate regions 18." For consistency of reference, these regions will be referred to herein as bases.

structure, since it was believed that the polygonal bases could well be dominated by corner effects with corresponding extreme (*i.e.*, spherical) junction curvature, and with it being impossible to include any closely spaced structure to reduce the electric field in those regions of high curvature. Moreover, Jambotkar's specially provided floating region adjacent to the bases teaches away from the two-dimensional base array described in the '725 patent.

These references thus make clear why the Okabe co-inventors, when addressing in their IEEE article the need to improve channel width in power MOSFETs, avoided the two-dimensional array of the Okabe low-voltage JFET -- the conventional wisdom at the time was that power MOSFETs should minimize bases with curved junctions, particularly spherical junctions such as would be found at the corners of polygonal bases. All of the references that specifically address power MOSFETs either use an inwardly conducting annular (or a single frame base) with *inwardly* conducting channels or employ some special diffusion to support the drain voltage in the off condition. No reference -- except the '725 patent -- suggests that it is desirable or even possible to employ polygonal bases (with *outwardly* conducting channels and junctions with spherical curvature) with no special structure to support the drain voltage when the device is turned off.[7]

The Okabe reference, in contrast, describes a configuration for arranging gate regions in a JFET designed to operate with about 8-10 volts across the device in the off condition -- indeed, the Okabe reference recites that it was **undesirable** to have to increase the drain-to-gate voltage beyond this magnitude in order to achieve pinch-off. (USPTO Trans., pp. 2, 3.) It is understandable, therefore, why the Okabe co-inventors included no discussion or analysis of the breakdown voltage performance of the Fig. 2 "conventional" FET device -- characteristics (as two of those co-inventors expressly recognized in their simultaneous IEEE article) essential to the design of a high power MOSFET. In the Okabe

[7] Three power MOSFET references of record employ a base with an outwardly conducting channel -- Takakuwa Figure 3/4, Jambotkar and the Lidow et al. '699 patent. In each reference, the designer included a specific annular structure spaced away from the base -- Takakuwa had JFET ring diffusion 17, the '699 central polygonal base had a surrounding annular base, and Jambotkar had a floating guard ring. Such surrounding annular structures, of course, are completely incompatible with replicating the bases in an array.

reference, they were unconcerned with operation where breakdown is a design issue, as is the case for power MOSFETs.

V. THE TIHANYI AND SAKAI REFERENCES DO NOT SUGGEST ALTERATION OF OKABE TO ARRIVE AT THE '725 INVENTION.

In the 5/17/95 Office Action, pages 10-11, the Examiner states that the "Okabe et al. MOSFET is similar in many respects to Sakai '688 MOSFETs of Figures 5 and 6 . . . and the Tihanyi et al. MOSFET of Figure 5 . . ." The Examiner goes on to conclude that the rotational or mirror image symmetry is "similar" to the symmetry of the "conventional MOSFET layout shown in Okabe et al. with Figures 1 to 4 . . ." (5/17/95 Office Action, pp. 11-12.) The Examiner then rejects certain claims based on the supposed motivation (1) to convert *each side* of the Tihanyi or Sakai bases into a polygonal base with rotational symmetry and (2) to replicate these modified bases into a two-dimensional array supposedly suggested by Okabe, with the high voltage performance of the resulting structure "inherent" in the (modified) Sakai base structure. (5/17/95 Office Action, pp. 10-13.)

For the reasons set forth above, Patent Owner respectfully traverses this rejection. The presumed MOSFET of Okabe Figure 2 contains base regions that, as the Examiner concedes, have inner channels only and hence are not designed for use in a symmetrical array. The Sakai and Tihanyi bases also have inwardly conducting channels only (*i.e.*, they are annular or an elongated annulus) and are for the same reasons ill suited for replication in an array.

Nor would those of skill be motivated to modify the Sakai or Tihanyi bases in the manner suggested by the Examiner. As discussed above, the conventional wisdom at the time of the Okabe reference and prior to the '725 invention was to avoid bases with curved MOSFET junctions, particularly spherical junctions such as would be found at the corners of polygonal bases. Accordingly, the references specifically addressing power MOSFETs generally provide for conduction into a drain pedestal or pedestals surrounded by a single annular or frame-shaped base. The Tihanyi and Sakai references are but further examples of

this conventional wisdom -- with inward conduction to a centrally located drain pedestal. Accordingly, neither Tihanyi nor Sakai would have been literally turned inside out -- departing from the conventional wisdom -- in order to transform the *inwardly* conducting FET of Okabe Fig. 2 into the *outwardly* conducting MOSFET device envisioned by the Examiner.

Thus, Patent Owner respectfully submits that there is no suggestion in Tihanyi or Sakai to warrant their combination with Okabe as proposed by the Examiner. Specifically, Tihanyi's discussion (on which the Examiner relies) of a plane of symmetry or a line of rotational symmetry within a central drain necessarily applies to an annular base or to an elongated base with an inwardly conducting channel. Tihanyi neither depicts nor suggests the possibility of a symmetrical base with a channel on its *outer* periphery, which would necessarily require corners forming spherical base-drain junctions prone to avalanche breakdown. Such a base would be essential to the symmetrical array hypothesized by the Examiner, yet there is nothing in Tihanyi suggesting that the conventional wisdom could be flouted in that manner.

VI. SECONDARY CONSIDERATIONS COMPEL A CONCLUSION THAT CLAIMS 1-14 AND PROPOSED NEW CLAIMS 15-26 OF THE '725 PATENT ARE UNOBVIOUS FROM THE ART

"Objective evidence of nonobviousness must always when present be considered en route to a determination [of the question] of obviousness because: 'evidence of secondary considerations may often be the most probative and cogent evidence in the record. It may often establish that an invention appearing to have been obvious in light of the prior art was not. It is to be considered as part of all the evidence, not just when the decision maker remains in doubt after reviewing the art.'", Uniroyal Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1053 (Fed. Cir. 1988), cert. denied, 488 U.S. (1988).

In the present case, a number of secondary considerations are present. Those considerations have been discussed in the Patent Owner's prior submissions. At this time,

therefore, Patent Owner will simply reiterate the tremendous advance in the performance-to-cost ratio permitted by the '725 invention, which in turn led to its remarkable commercial success.

As previously noted, a key design objective for a power MOSFET is to maximize the channel width per unit area of the chip or die. This is because, for a given breakdown voltage, the on-resistance is inversely related to channel width (*i.e.*, the larger the channel width, the lower the on-resistance), while the cost of the die is generally directly proportional to its area.

To give some perspective, the Yoshida IEEE article reports that the design described therein achieved 94 cm of channel width on a 5 mm x 5 mm chip, or a channel width per unit area of a little less than 38 mm^{-1}. The '725 patent reports that a design according to that invention achieved 22,000 mils of channel width on a 100 mil x 140 mil chip, or a channel width per unit area of about 62 mm^{-1} -- an improvement of more than 64% over the Yoshida design.

The improvement is even more dramatic when compared to Patent Owner's prior art design (as depicted in the '286 patent): As set forth in the accompanying Declaration of Alexander Lidow, the '725 invention permits a three-fold increase in on-state performance for a given die area. Thus, the '725 patent permits on-resistance to be lowered by 2/3 as compared to a MOSFET having the same voltage rating and die size but using the prior-art topology. Alternatively, the same performance (in terms of on-resistance and breakdown voltage) as a prior-art design can be achieved with only 1/3 of the die size -- which translates into 1/3 of the cost -- of a prior art device. Lidow Decl. ¶¶ 6-7.

This dramatic improvement in the performance-to-cost ratio made power MOSFETs a cheaper but technically superior alternative to bipolar transistors for many power applications, and rendered obsolete all prior power MOSFET designs. Power MOSFETs filled only a small niche of the power semiconductor market in 1979, when the first MOSFETs practicing the '725 invention were introduced. Today, power MOSFETs

make up nearly 50% of the total market for power semiconductors -- representing nearly $1 billion in power MOSFET sales last year -- and virtually all of these MOSFETs practice the '725 invention. Lidow Decl. ¶¶ 8-9.

VII. CONCLUSION

For all the above reasons, it is requested that the Examiner confirm the patentability of claims 1-14 and of proposed claims 15-26 of U.S. Patent 5,008,725.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on June 27, 1995:

Stephen A. Soffen
Name of applicant, assignee or Registered Representative

Signature

June 27, 1995
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Respectfully submitted,

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<u>CERTIFICATE OF SERVICE</u>

The undersigned hereby certifies that a true and correct copy of the foregoing "RESPONSE PURSUANT TO 37 C.F.R. § 1.550(b)" is being served on the attorneys for Requester SGS-Thomson Microelectronics, Inc. by sending a true copy of such document by first class mail, postage prepaid, on June 27, 1995 to the address set forth below.

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AMDT\121630

OFGS File No.: IR 2.064 (2-838)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:

ALEXANDER LIDOW et al.

Patent No.: 5,008,725

Reexamination Control No.: 90/003,495

Filing Date: July 15, 1994

Examiner: CARROLL, J.

Group Art Unit: 2508

DECLARATION OF JOHN SHOTT

I, John Shott, declare as follows:

1. I received my B.S. (1972), M.S. (1972) and Ph.D. (1978) degrees, all in Electrical Engineering, from Stanford University. I am presently a Senior Research Associate of Stanford University. I have been employed in various research positions at Stanford for over 20 years. I am an expert in microelectronics and semiconductor fabrication techniques, and in particular the fabrication of semiconductor

8. If the base of a vertical MOSFET is formed through a square or rectangular diffusion window, then one would expect the depletion layer to be thinnest at the corners, and avalanche to occur at the corners before the sides or bottom of the junction. Thus, the breakdown voltage of the device is limited by the reduced breakdown voltage at the corners of the base-drain diffusion window. On the other hand, if the junction was formed by an annular diffusion similar in shape to that described in Paragraph 5, above, then the depletion layer would be thicker at the corners than at the edges, and the edges would define the point at which avalanche breakdown occurred. In other words, for two otherwise identical junctions, the junction with a square surface expression will break down at a lower voltage than a junction with an annular surface expression.

9. Prior to the invention of the '725 patent, those of ordinary skill in the power MOSFET art generally analyzed breakdown voltage by considering the reverse-biased junction and typically made use of the foregoing principles when estimating the effects of junction shape on breakdown voltage.

10. It is for this reason that the conventional wisdom prior to the '725 invention was to avoid base regions with outwardly conducting channels and to avoid structures with sharp corners that would produce spherical junction curvature, which would have relatively thin depletion layers at the corners of the diffusion windows. Wider depletion layers, and hence better breakdown performance, all other things being equal, were felt to occur with annular or frame bases.

11. The '725 patent defied this conventional wisdom by deliberately using polygonal bases having essentially spherical junctions at each corner. That the breakdown voltage of the resulting structure was not degraded was a surprising result of the invention.

12. I am aware of two references from about the time of the '725 invention that address the electric-field or breakdown-voltage effects of one junction on a nearby junction. These are U.S.Patent No. 4,055,884 to Jambotkar (filed December 13, 1976) and U.S. Patent No. 4,206,469 to Hanes et al. (filed September 15, 1978). In each of these references, the designer sought to improve breakdown voltage of a long, straight junction (*i.e.*, a junction with cylindrical curvature) by opposing that junction with a closely spaced junction of the same curvature. Both references emphasize that these opposing cylindrical junctions must be closely spaced and parallel in order to result in reduced electric field strengths in the curved portions of the junctions.

13. Neither Hanes nor Jambotkar suggests the structure or result of the '725 invention. Both of those references relied on closely spaced, parallel junctions with *cylindrical* curvature. The '725 patent, on the other hand, deliberately introduces junctions with *spherical* curvature, which was known to increase electric field strengths when reverse-biased and hence to lower the breakdown voltage of the junction. In my opinion, the ability of the polygonal bases described in the '725 patent to maintain adequate breakdown voltage performance was an unexpected and surprising result.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on June 27, 1995 at Stanford, California.

John Shott, Ph.D.

OFGS File No.: IR 2.064 (2-838)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:

ALEXANDER LIDOW et al.

Patent No.: 5,008,725

Reexamination Control No.: 90/003,495

Filing Date: July 15, 1994

Examiner: CARROLL, J.

Group Art Unit: 2508

DECLARATION OF
ALEXANDER LIDOW

I, Alexander Lidow, declare as follows:

1. In late 1978, power MOSFETs were manufactured and sold by International Rectifier which used the topology generally disclosed in Figure 1 of Patent 4,376,286, which is hereinafter termed a "serpentine path." MOSFET products using the serpentine path topology were sold in 1978 and 1979, and received a very enthusiastic market reception, as described in my earlier declaration dated March 23, 1995.

2. The 400 volt version of the device with a serpentine path was designated by the type number IRF 305. This device had an on-resistance of 1 ohm and had a silicon chip area of 250 mil x 270 mil. While this device represented a dramatic improvement over power MOSFETs not practicing the '286 invention, it still required a relatively large die and accordingly cost more to manufacture than an otherwise equivalent bipolar transistor.

3. At about the time the IRF 305 reached the market, I and my co-inventors Herman and Rummenik made the invention of Patent 5,008,725 which, for convenience, is term a "multicellular geometry," rather than the serpentine path geometry of the '286 patent. The concept of the multicellular geometry using spaced base cells caused a dramatic and unexpectedly large increase in channel width per unit areas of silicon as compared to that of a serpentine path geometry, without compromising the breakdown voltage of the device.

4. The cost of a power MOSFET semiconductor chip is highly related to its silicon area. The performance of the chip is directly related to its channel width, which in turn is inversely related to on-resistance (*i.e.*, the larger the channel width, the lower the on-resistance). In order to get the most performance for a given chip size (*i.e.*, cost), MOSFET designers attempt to maximize channel width per unit area while maintaining the required breakdown voltage.

5. Because the multicellular geometry was so superior in channel width per unit area, and did not compromise the breakdown voltage of the device, we immediately made plans to, and did, replace the IRF 305 device by devices using the multicellular geometry.

6. One new product (in 1979) using the multicellular geometry was the part type IRF 330 which was a 400 volt device having an on-resistance of one ohm (like that of the IRF 305), but a chip area of only 175 mil x 130 mil. This is approximately one-third the area of that of the equivalent serpentine path IRF 305. Thus, IR's cost for this chip was reduced by approximately 2/3, enabling its ultimate reduction in market price to one more competitive with that of bipolar power transistors of similar power-handling capability.

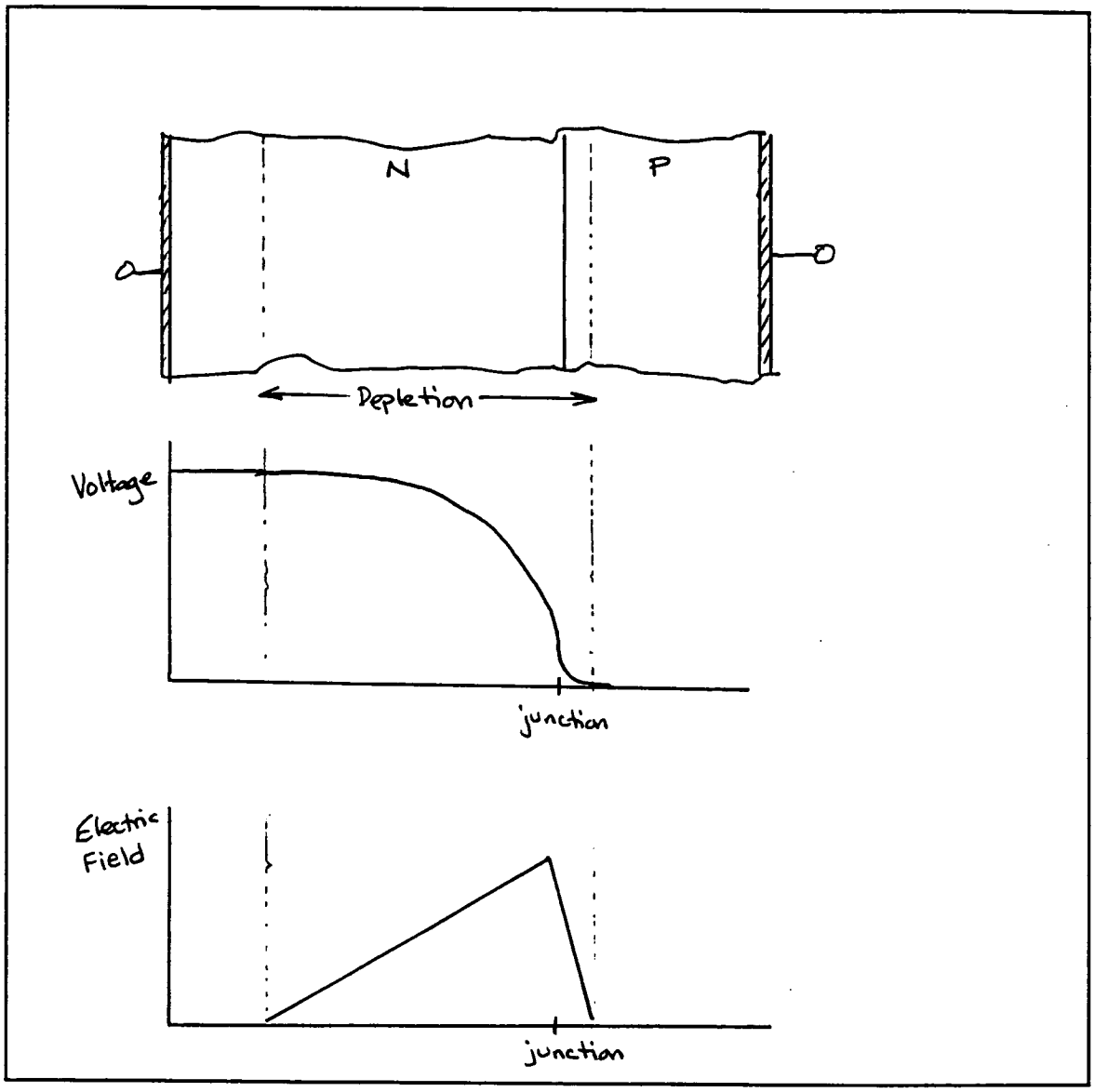
7. Another new product (in 1979) using the multicellular geometry was the part type IRF 350. This part kept the same die area as the IRF 305, but its on-resistance was reduced to 0.3 ohms, an approximately three-fold reduction from that of the 1 ohm IRF 305 without a change in manufacturing cost. The reduction in on-resistance made the part more competitive with the performance of the traditional bipolar transistor for that voltage rating.

8. The cellular topology therefore made the International Rectifier power MOSFET more directly price competitive with the bipolar transistor over a broad spectrum since it permitted either a reduced on-resistance for a given die size or the same on-resistance for a much smaller die area.

devices employing metal-oxide-semiconductor (MOS) and/or bipolar technologies. I was qualified, and testified, as an expert in MOS technology in the 1989-90 trial of International Rectifier Corporation vs. Siliconix Incorporated, Case No. CV 86-4198 R (C.D. Cal.), which involved a series of IR patents that described and included claims covering power MOSFET structures, including U.S. Patent Nos. 4,376,286, 4,642,666, 4,705,759, 4,680,853 and 4,593,302. I also testified as an expert witness in the 1993-94 evidentiary hearing in International Rectifier Corporation vs. SGS-Thomson Microelectronics, Inc., Case No. CV 90-4802 R (C.D. Cal.), which involved SGS-Thomson's infringement of IR's power MOSFET patents 4,642,666 and 4,959,699.

2. As is well known in the semiconductor art, when a p-n junction is reverse biased, electrical forces will move electrons in the n type region away from the p-n junction and similarly will move holes in the p type region away from the junction, thus forming a "depletion region" with virtually no free electrons or holes available for conduction. The electric field within the depletion region will be essentially zero at the edges of the depletion layer, and (assuming uniform doping) will increase linearly to a maximum value at the p-n junction. As shown in the following sketch, the voltage will start at the potential applied to the n type region and will remain at that potential until the edge of the depletion layer. At this point, the potential will fall in a quadratic (or square-law) fashion until the junction is reached, at which point the curvature (*i.e.*, the second derivative) of the voltage curve changes polarity and the voltage will reach 0 at the edge of the depletion layer in the p type region. If the n type region has much less dopant than the p type region,

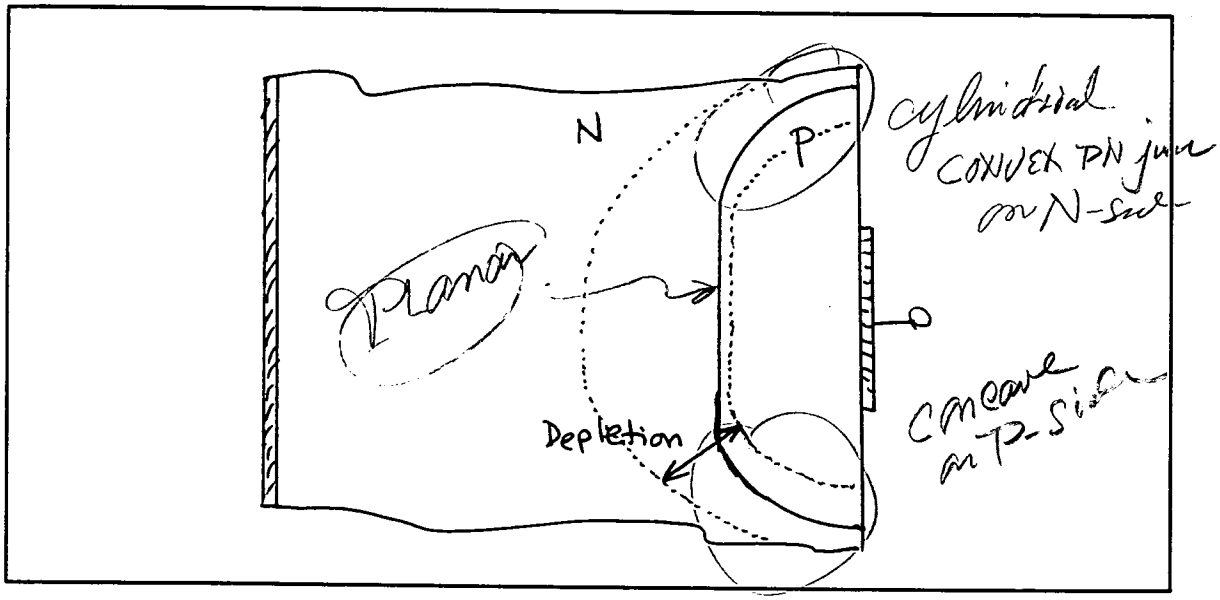
the depletion region is much wider on the n side; most of the potential will be dropped across the n side of the junction; and the potential will vary gradually through this region.



Voltage distribution and depletion layer for reverse biased planar junction with n type dopant concentration of $2x10^{14}$ and p type dopant concentration of $2x10^{17}$.

3. Since all semiconductor junctions have a finite size in all three dimensions, as a next analytical step, it is useful to consider a junction formed by diffusion

through a stripe -- *i.e.*, a junction having a finite depth and which is limited in one lateral dimension. The resulting junction can be thought of as having a planar section and two edge sections (each representing one-quarter of a cylinder). Because the curved junctions result in a narrower depletion region where the junction is convex (see sketch), both the average and the peak electric field in those portions are higher than in the corresponding planar portion.



Depletion region in reverse biased junction with cylindrical corners and doping concentrations in p region much higher than doping in n region (note depletion width is not drawn to scale).

The depletion layer becomes thinner where the junction defines a convex surface because it is essentially balancing carriers on both sides of the junction. When the junction is *convex* (such as for the n region in the curved portions, above), the layer needed to capture a given number of carriers is thinner than that needed for a planar junction surface. Conversely, when the junction is *concave* (such as for the p region in the curved portions, above), the

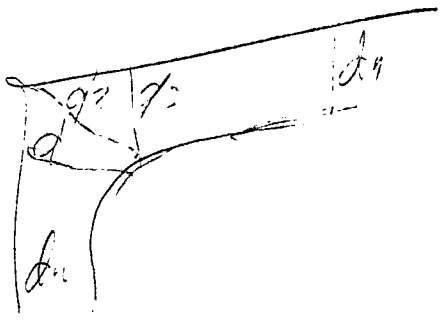
layer needed to capture a given number of carriers is thicker than that required for a planar junction surface.

4. The shape of the diffused region in a semiconductor device, when viewed from the top surface, can have significant effects on depletion regions formed in connection with the reverse-biased junction. When the diffusion window used to form the junction is a rectangle or square, it will have four corners that will create junction shapes that are essentially spherical -- *i.e.*, they are curved in two dimensions. The region on the convex side of the junction needed to capture a given number of carriers will be thinner in the spherical portion than that needed for the cylindrical junctions discussed above, and will be much thinner than that required for a planar junction. Thus, for a junction formed by diffusion through a square or rectangular window, the depletion layers when the junction is reverse biased will be thickest in the center of the window (*i.e.*, at the bottom of the junction, where it is essentially planar), thinner along the edges (where the junction is essentially cylindrical -- *i.e.*, curved in one dimension) and thinnest at the corners (where the junction is essentially spherical -- *i.e.*, curved in two dimensions).

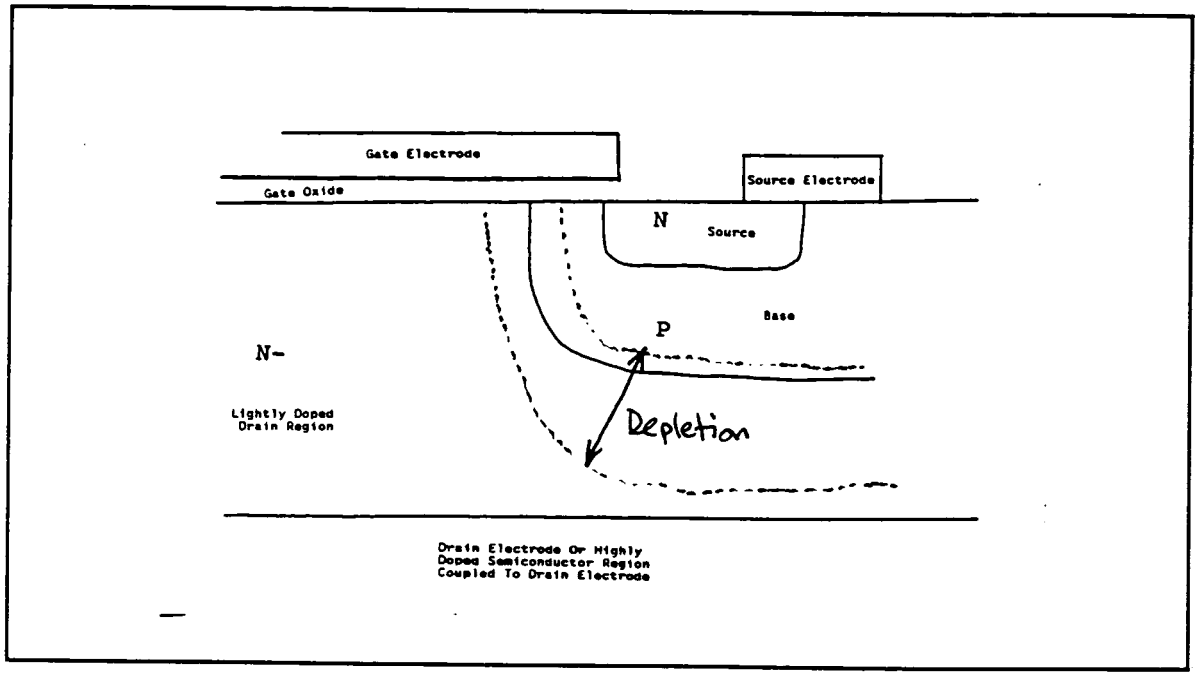
5. If, however, the junction is formed by diffusing dopant into an annular shape (such as where diffusion occurs over the entire surface of the device except for a central square region), then the junction curvature at a corner of the central region will have one component that is cylindrical (with concave curvature) and another component that has an offsetting (*i.e.*, concave) curvature, so that the region on the convex side of the junction needed to capture a given number of carriers is thicker than for a cylindrical

junction and approaches the thickness of the corresponding region for a planar junction. In this configuration, the depletion layers at the bottom and at the corners of the junction will be of comparable thickness, with the thinnest depletion layers along the edges of the central region.

6. The following sketch illustrates a depletion layer in a vertical MOSFET in the off condition at a cross section remote from any corners of the diffusion window. Note that, because the base is highly doped compared to the lightly doped drain, the depletion layer is predominantly in the drain region. Also, in accordance with the foregoing discussion of curved junctions, the depletion layer in the drain becomes thinner



along the edge of the diffusion window, where the base region curves upward toward the surface.



Depletion layer in hypothetical vertical-conduction MOSFET when device is turned off and base-drain junction reverse-biased (not to scale). OFF-State

7. "Avalanche" breakdown of a vertical MOSFET occurs when the maximum electric field (which occurs at the p-n junction) exceeds a critical value. As reverse bias is increased, the maximum electric field builds up and eventually reaches a critical value at which avalanche occurs. Under suitable conditions, it is frequently reasonable to approximate this maximum electric field of a reverse-biased junction as twice the applied voltage divided by the depletion width. Thus, the wider the depletion layer, the lower the maximum electric field, and the higher reverse bias that may be applied to the junction before the maximum electric field reaches a critical value and avalanche occurs.

9. The dramatic improvement in the performance-to-cost ratio permitted by the '725 invention made power MOSFETs a cheaper but technically superior alternative to bipolar transistors for many power applications. Power MOSFETs filled only a small niche of the power semiconductor market in 1979, when the first MOSFETs practicing the '725 invention were introduced. Today, power MOSFETs make up nearly half of the total market for power semiconductors -- representing nearly $1.5 billion in power MOSFET sales last year -- and virtually all of these MOSFETs practice the '725 invention.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on June 27, 1995 at El Segundo, California.

Alexander Lidow